**DESIGN AND VERIFICATION OF 8-BIT SERIAL IN PARALLEL OUT SHIFT REGISTER**

**ABSTRACT:**

This project involves in designing and verification of 8 bit SIPO shift register .In the **"Serial IN Parallel OUT"** shift register, the data is passed serially to the flip flop, and outputs are fetched in a parallel way. The data is passed bit by bit in the register, and the output remains disabled until the data is not passed to the data input. When the data is passed to the register, the outputs are enabled, and the flip flops contain their return value.This project aim is to verify the sipo shift register with System Verilog testbench.

**EXPECTED OUTCOMES:**

The primaryoutcome is to implement the SIPO register using Verilog in design.

Successful verification and validation of SIPO register is done using System Verilog Testbench Architecture.

SIPO register is mainly used to

1. Generate time delays in digital logic circuits
2. Transfer and store data
3. Reduce the number of wires connecting different systems in a design
4. Store and retrieve data in applications where serial transmission is more efficient or feasible